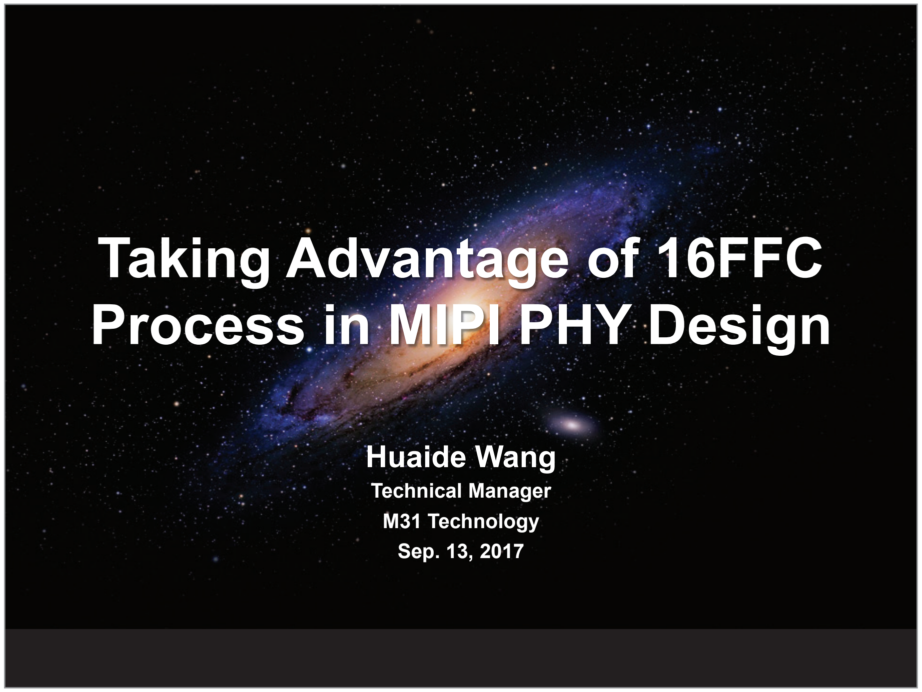
Taking Advantage of 16FFC Process in MIPI PHY Design

M31 Technology

ABSTRACT

As the MIPI standards are more mature in these years, MIPI interfaces, including D-PHY, C-PHY, and M-PHY, become more popular in different area. The requirement does not only come from mobile communication, automobile and home-safety system also bring new chance. A common feature of these emerging applications is they all need complexity algorithm, which will be more efficient in modern process, such as 16FFC.

In this presentation, we will compare the advantage that we can utilize from 28HPC to 16FFC process. With the process shrinkage, the leakage control and ESD protection should be taken into serious consideration. Also, since the supply voltage decreases, the power-supply noise rejection performance becomes more important. After the challenge analysis, we will show our solution of M-PHY TRx and C/D-PHY combo TRx design. The power efficiency is almost improved by twice compared with the previous version.



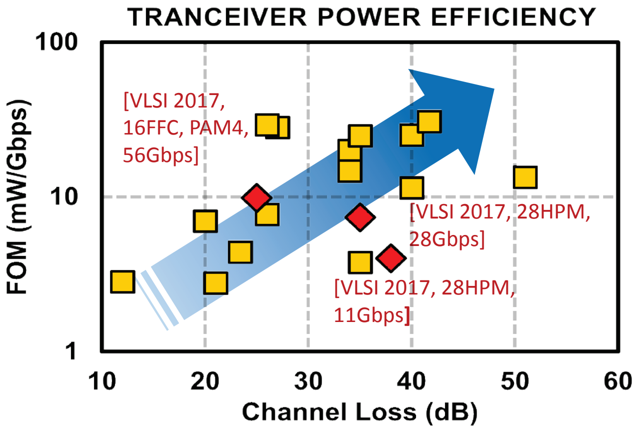
Outline

- MIPI Development Status
- Benefit & Challenge from FinFET Process
- Deep Thinking in MIPI Design
  - M-PHY
  - C-PHY & D-PHY
- Summary

MIPI Application Evolution

- MIPI becomes hot in different area with everything smart.
  ➔ Smart phone, Smart watch, Smart Car, Smart home.

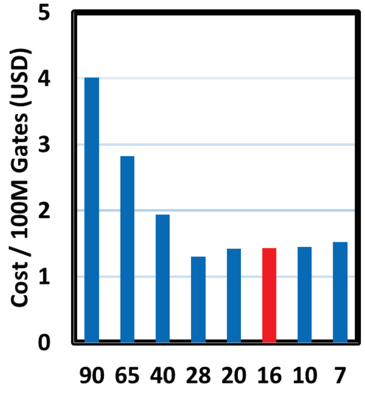
Transceiver Development Status



- Designers try to do better than the trend line: 10X FOM / 20dB
  - Using dynamic circuit instead of constant-current.
- FinFET process is widely adopted in complex applications.

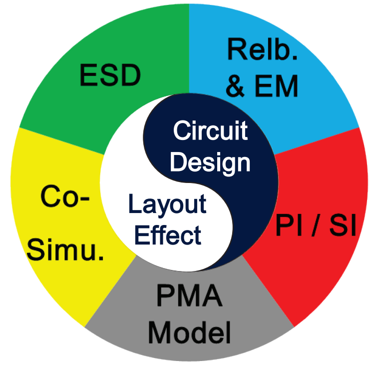
Design Cost & Strategy

➢ **Design Cost**



[REF] IBS, Inc.

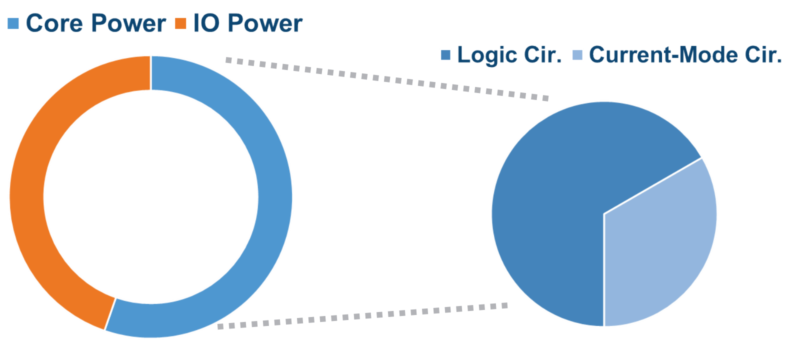
➢ **Design Effort**



➢ **Serdes IP becomes more sensitive to environment and put more effort on early-stage system validation.**

Benefit & Challenge from FinFET Process

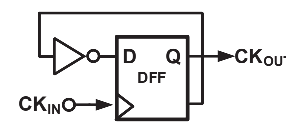
M-PHY Transceiver Power Budget



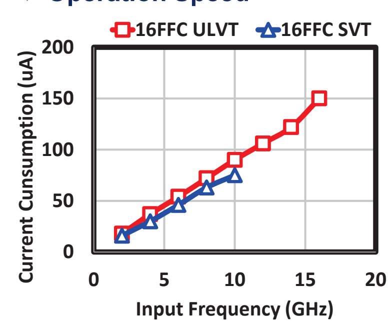
- ➢ **Core Power:**
  - ➢ **SER/DES, TX Driver, RX Front-End**
- ➢ **IO Power:**
  - ➢ **Clock Distribution, PLL**
- ➢ **Logic Circuit:**
  - ➢ **SER/DES, Divider, Sampler**
- ➢ **Current-Mode Cir.:**
  - ➢ **Driver, RX Front-End**

Digital Power Reduction – Standard Cell

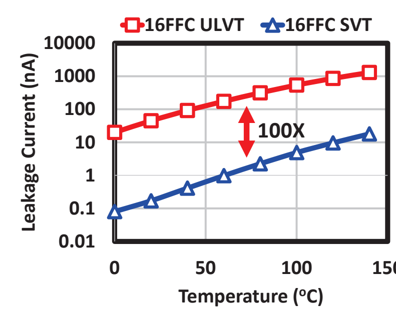
- ➢ **uLVT devices provide 1.5 X operation speed while the leakage is 100X.**
- ➢ **Power-gated technique also becomes more important for analog design.**



➢ **Operation Speed**

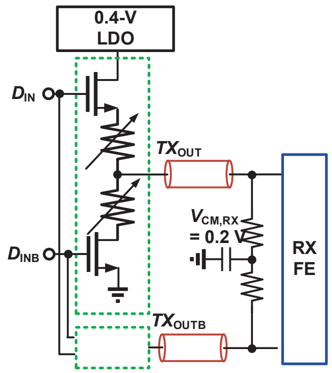


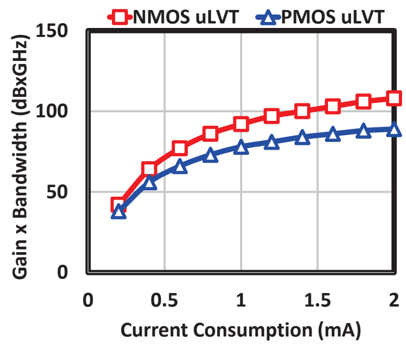
➢ **Leakage Current**



Analog Power Reduction - CML Buffer

- M-PHY Link Illustration
- 16FFC CML Buffer Performance

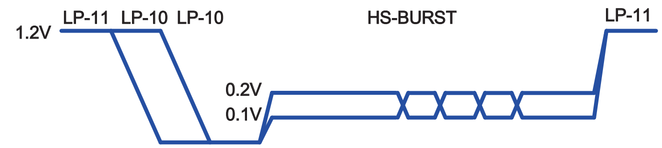


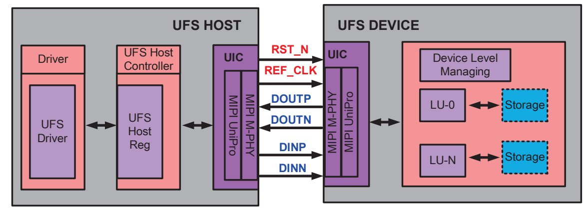


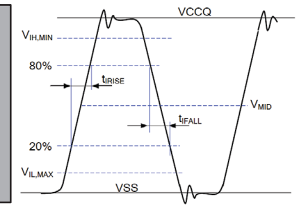
- All C/D/M-PHYs are required to support near-ground input level.
- 16FFC provides better symmetric performance in NMOS/PMOS under 6-Gbps operation.

IO Power Reduction

- C-PHY & D-PHY need 1.2-V for low-power data transmission.
- M-PHY needs RST_N & REF_CLK pins for UFS applications.
  - Extra LDO with capability of providing huge transient current.

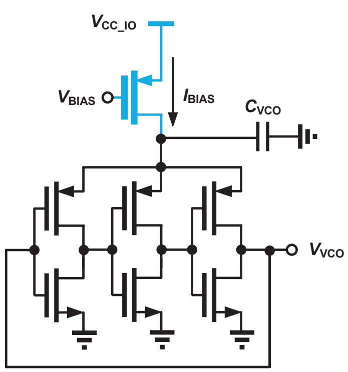




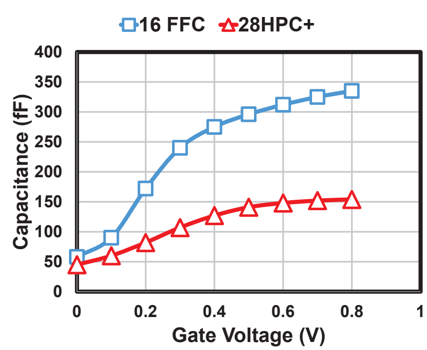


IO Voltage Reduction for PSRR

- PSRR is proportional to headroom: $I_{BIAS}/(V_{GS}-V_{TH})$
  - V_{TH} improvement from uLVT & IO devices totally save 350 mV.
  - 16FFC has 2x capacitance per area.

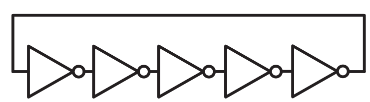


- Varactor Capacitance



Flicker Noise – FOM of VCO

- A 5-Stage Ring-Oscillator

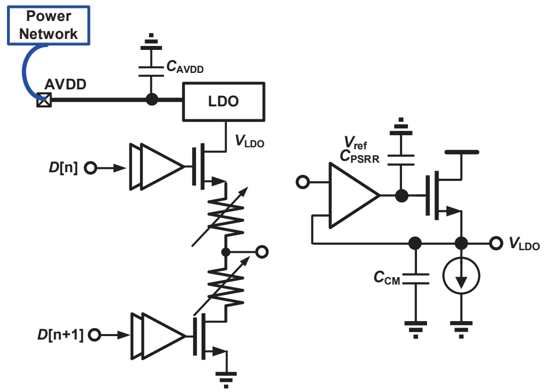


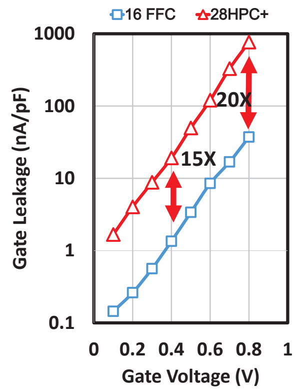
$$FOM = \frac{\sqrt{I}}{f_{osc}} \times 10^{\frac{PN@1MHz}{20}}$$

Process	PN @ 1MHz	Flicker Noise (%)	Current (uA)	FOM	PN Ratio	MOS Size (um^2)
28HPC+	91.7	71	550	2.1e-16	1:1	2.5
16FFC	93.5	98	520	1.6e-16	3:1	2.1

- 16FFC could not get too much benefit from FOM:
  - Burning power for decreasing flicker noise.
  - Area is also almost the same.

MPHY Transmitter Driver Design

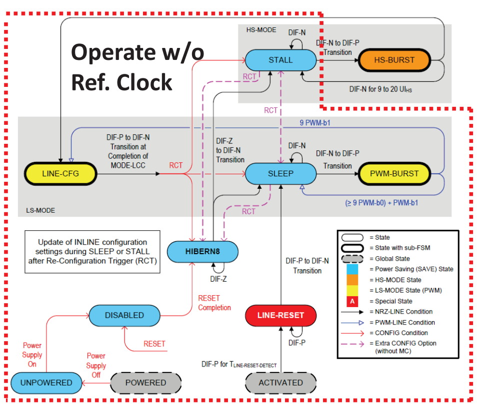


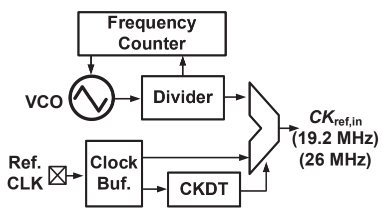


- ➢ TX gets benefit from driver sizing & capacitance density.
- ➢ The leakage current per unit capacitance of 16FFC is 1/15~1/20 of 28HPC+.

Deep Thinking in MIPI Design

Self-Clock Design in M-PHY Device



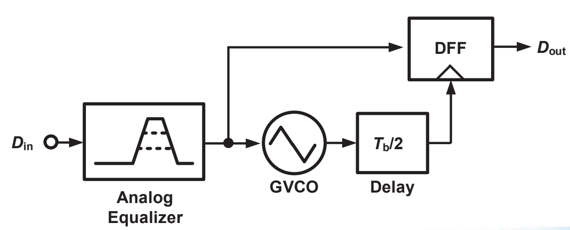


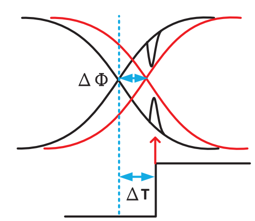
- ➢ In UFS, the receiver may support self-clock in HIBERN8, SLEEP, and PWM-BURST.
- ➢ M31 provides a pseudo reference in device mode.

CDR Architecture for Fast-Locking

- ➢ Adopting GVCO to meet LLI operation requirement.
  - ➢ Prepare < 5 SI, Sync Length < 32 SI (M31's spec is within 8 SI.)

	Locking Time	Power	Design Complexity
Gated-VCO	🙂 🙂	🙂	😐
Injection-Locking	🙂	🙂	☹️
PI/PLL-Based	☹️	😐	🙂

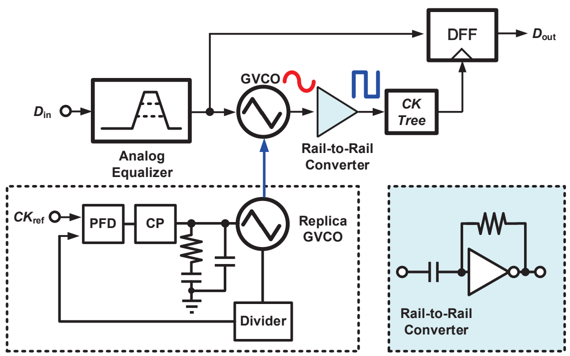


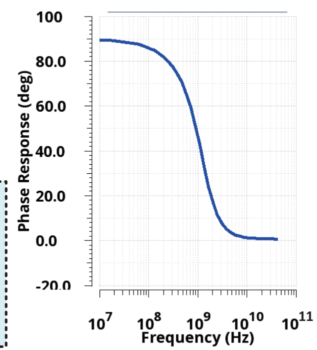


EDA Track
IP Track
EDA / IP / Services Track
Print-Only Papers

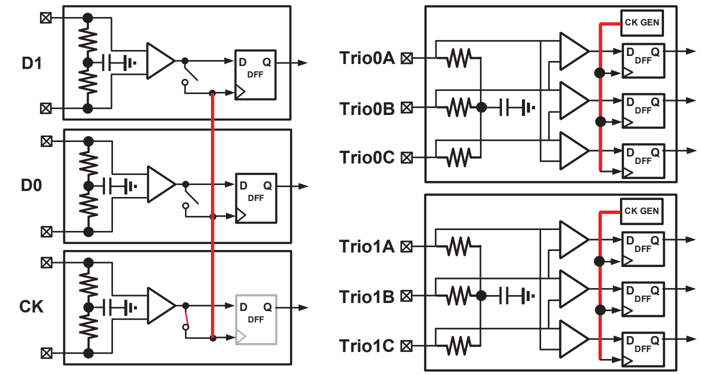
Detail of GVCO-Based Burst-Mode CDR

- Challenge:
  - Delay mismatch from rail-to-rail converter & clock tree.
  - Need PLL/FLL loop to track the frequency offset .





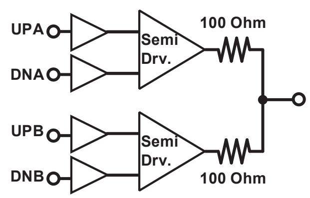
Flexible C/D-PHY Combo Design



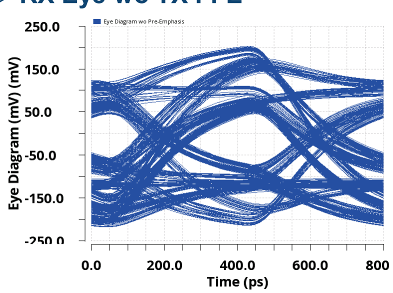
- Lots of switch option: Input termination, input buffer, clock tree…
- M31 provides more possible flexibility:
  - D-PHY data & clock lane swapping.
  - C/D combo Rx provides 4 Trio in CPHY or 4D1C or 2D1C*2 in DPHY.

C-PHY TX Pre-Emphasis

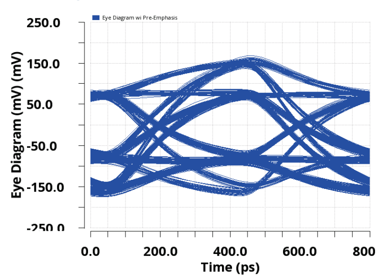
- C/D-Combo TX is complex to support Type-I/Type-II & pre-emphasis.
- Beyond 2.5 Gbps, TX FFE becomes must for C-PHY.



- RX Eye wo TX FFE

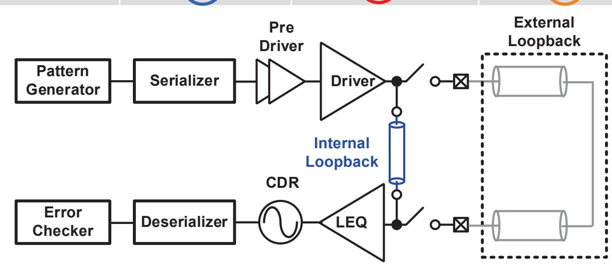


- RX Eye wi TX FFE



At Speed Loopback – M-PHY

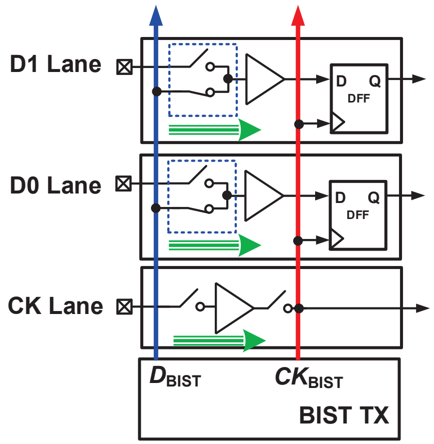
	Flexibility	Design Effort	Testing Cost
External LB	😊	😊	☹
Internal LB	😐	☹	😊



- External loopback could be very sensitive, especially in CP stage.
- M31 provides full function test in internal loopback, including line-state detector & programmable sensitivity testing.

At Speed Loopback – C/D-PHY

- **For RX, we implement a cost-effective built-in TX.**
  - Programmable sensitivity & operation speed.
  - Solve data & clock skew between normal & internal loop-back path.
  - Fully test all high-speed path with C-PHY & D-PHY pattern.
- **For TX, we have partial internal loopback to verify at-speed timing block.**
  - Leave driver for DC testing to simplify design.



Summary

- **MIPI takes place from mobile to automotive, and even digital home in display & storage.**
- **16 FFC does not only saves both core digital & analog power but also provides possibility to reduce IO voltage.**
- **Along with the increasing cost, the design procedure becomes more strict. PMA Verilog model, reliability & EM, and PI/SI analysis become necessary.**
- **The design in MIPI may need more than spec., such as internal loopback, locking-time reduction, and TX pre-emphasis.**

M31 Mobile Interface IP Status

Mobile IP Category	Proven Process	2017			2018	
		Q2	Q3	Q4	Q1	Q2
M-PHY V4.0	On-going				16/12FFC	
M-PHY V3.0	28HPC/40LP/55LP					
D-PHY V1.2	On-going	28 HPC+			16/12FFC	
D-PHY V1.1	28HPC/40LP/40ULP/55LP	28 HPC+			16/12FFC	
C/D-PHY Combo	On-going	28 HPC+			16/12FFC	

M31, The source for Evolutionary IP

Thank You

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